ACQ494FMC
Preliminary Product Specification

High Performance Simultaneous Data Acquisition

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1 Product Description

1. ACQ494FMC is an 4 channel time to digital converter (TDC).
2. VITA 57 FMC module, LPC compliant.
3. Single Pin LEMO LVCMOS compatible Inputs.
4. Compliant with D-TACQ *ELF* sites. When shipping exclusively in D-TACQ carriers, may ship as cost-reduced ACQ494ELF build variant

1.1 Product Variants

1.2 Overview

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with a dual-core ARM Cortex A9 and gigabit Ethernet.

Compatible carriers include:

- D-TACQ **ACQ1001** : D-TACQ single slot FMC carrier, Z7020
- D-TACQ **ACQ1002** : D-TACQ dual slot FMC carrier, Z7020
- D-TACQ **ACQ2106** : D-TACQ 6 slot FMC carrier, Z7030

Note: Compatibility with ACQ1001/1002 is limited as these carriers do not support White Rabbit for precision timing.

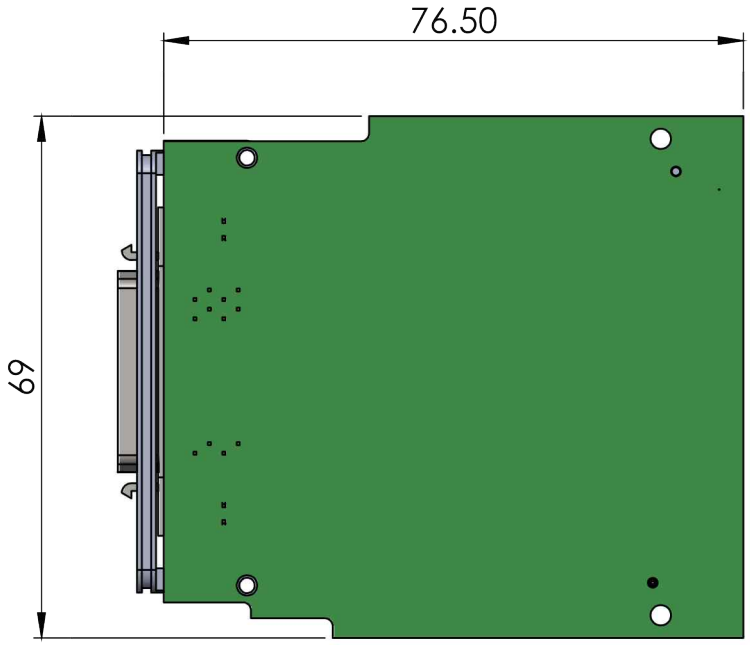
D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux. Evaluation boards are useful for evaluation, but for production use D-TACQ recommends use of a production-quality carrier such as ACQ2106.

1.3 Glossary

- *FMC*: VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ Soc
- *FPGA* : Field Programmable Gate Array.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC*: *FMC* Ultra low pin count (D-TACQ).
- Extended, ELF : *FMC* Extended size module (D-TACQ).
- TDC Time to Digital Converter

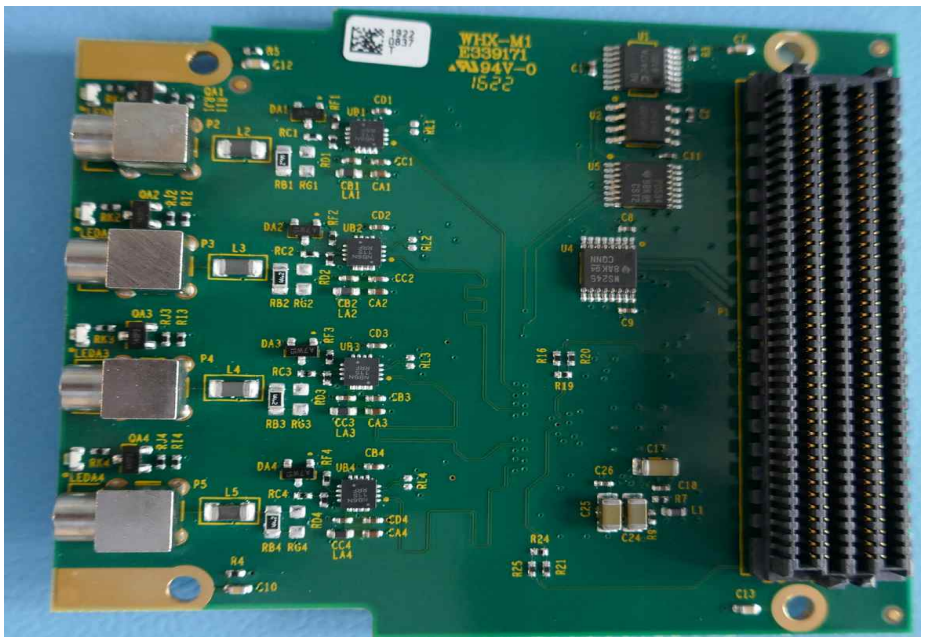
2 Physical

2.1 Dimensions



Standard FMC Module

2.2 Appearance



3 Interface Specification.

3.1 Front Panel Connectors

- 4 x MCX.
- Centre Pin Signal, shield 0V
- Alternative LVDS build option TBD

3.2 Electrical

3.2.1 Signal Input

- LVTTL compatible DC Coupled
- 50 Ohms / X kOhm Input Impedance. Software Selectable
- Alternative LVDS build option TBD

3.2.2 Input Receiver

TBD LVTTL to LVDS (preliminary choice is LMK1D2102 or NB4N855S)

Improved characteristics to CDCLVC1102PW (as used on CERN TDC board) as follows

	CDCLVC1102 @ 3.3V			LMK1D2102		
	Min	Typ	Max	Min	Typ	Max
Propagation Delay (nS)	0.8		2.0	0.3		0.575
Output Skew (pS)			50			20
Pulse Skew (pS)			180	-20		20
Part to Part Skew (pS)			500			250

3.2.3 TDC Converter

The Board uses the TDC-GPX2 Converter. All specification characteristics are driven by the performance of this device. In addition to this the following modes are used

- Input signals:
  - LVDS inputs using input receivers.
- Output signals to FPGA:
  - ACQ2106 LVDS signalling at up to the 250 MHz TDC-GPX2 maximum

4 ACQ494FMC TDC Specification (TDC-GPX2 Hi-Res off).

#	**Parameter**	**Value**
1	Number of Channels	4
2	Event Rate	Per channel asynchronous 12 MEvents/s
3	Mesurement Resolution	1pS
4	Accuracy	TBD Target <500pS
5	Precision	TBD
6		
7	Peak Conversion Rate	50 MSPS (16 Stage FIFO)
8	Maximum Continuous Readout Rate 8 bit Ref, 20 bit Delay	17 MSPS (per Channel)
9	Latency	20 nS
10	Pulse-to-pulse spacing	20nS
11	Pulse-to-Pulse Spacing in Channel Combine Mode, 2 Channels Combined	5nS
12	Input Pulse Width	> 2nS (TDC-GPX2 LVDS input)
13	Refclk Frequency	TBD (provisionally 10 MHz)
14		
15		
16		
17		

See the TDC-GPX2 datasheet for a full definition of the device.

5 ACQ494FMC Module Specification.

#	**Parameter**	**Value**
1	Form Factor	Standard FMC
2	Power source	External DC 12V, TBD mA External DC 3.3V, TBD mA
3	Environmental	0ºC-40ºC Operational -10ºC-85ºC Non-Operational
4	FMC Socket	Standard FMC, Low Pin Count LPC

6 FMC Connector Pinout

The ACQ420FMC module uses a LPC FMC connector with the following provisional pin out.

The Dedicated FMC I2C pins are used for I2C bus expansion features such as Termination Enable.

FMC Pin	**Signal Name**	**Description**
p_FMC_CLK1_M2C_p		REFCLK LVDS Pair
p_FMC_CLK1_M2C_n		
p_FMC_LA00_CC_p		LCLKOUT LVDS Pair
p_FMC_LA00_CC_n		
p_FMC_LA01_CC_p		LCLKIN LVDS Pair
p_FMC_LA01_CC_n		
p_FMC_LA02_p		SDO1 LVDS Pair
p_FMC_LA03_p		FRAME1 LVDS Pair
p_FMC_LA04_p		SDO2 LVDS Pair
p_FMC_LA05_p		FRAME1 LVDS Pair
p_FMC_LA06_p		SDO3 LVDS Pair
p_FMC_LA07_p		FRAME1 LVDS Pair
p_FMC_LA08_p		SDO4 LVDS Pair
p_FMC_LA09_p		FRAME1 LVDS Pair
p_FMC_LA10_p		RSTINDX LVDS Pair
p_FMC_LA11_p		REFCLK LVDS Pair (ALT)
p_FMC_LA12_p		PARITY
p_FMC_LA13_p		SPI SCLK
p_FMC_LA14_p		SPI MISO
p_FMC_LA15_p		SPI MOSI
p_FMC_LA16_p		SPI CS
p_FMC_LA17_CC_p		INTERRUPT
p_FMC_LA18_CC_p		
p_FMC_LA19_p		
p_FMC_LA20_p		SDO1 Monitor TBD
p_FMC_LA21_p		SDO2 Monitor TBD
p_FMC_LA22_p		SDO3 Monitor TBD
p_FMC_LA23_p		SDO4 Monitor TBD

7 FPGA Processing

This section is intended to describe the FPGA processing features supported for this module on the ACQ2106 Carrier. This is a provisional section.

The TDC-GPX2 Output format will be 8 bits of REFCLK and 20 bits of Stop Time. This gives the ability for the following mode of operation.

The FPGA tracks the number of REFCLK cycles per second. The 8 bits of REFCLK count from the TDC-GPX2 are combined with this for counter roll-over synchronous correction to form a 24 bit counter for the 10 MHz (100 nS fractional Time) . In addition to this a 2 bit “channel” and a 3 bit “site” field to encode which channel in which board (this logic allows for up to 6 TDC boards per ACQ2106)

This is rounded up to a 64 bit “event” to store each Event.

On every second (PPS) transition a TAI indicator of the current White Rabbit time is embedded in the datastream.

This allows full reconstruction of the time base for every event.

For a 4 channel system operating at the maximum event rate this equates to

4 channels x 12 MEvents/s x 8 bytes per event = 384 Mbtes/s which is well within the ACQ2106 maximum capture rate.

The data could also be sent to a external system over Xilinx Aurora Fibre Link to a Host PC or FPGA board for either large datasets or real time feedback.

The REFCLK Reset feature of the TDC-GPX2 would be used to ensure the REFCLK count is cleared every Second on the PPS signal to ensure minimum drift in time.

An alternative mode of operation would be a condensed data mode. Here the Stop time is condensed to 18 bits, the REFCLK to 9 bits and the Event then occupies 32 bits. This requires both a TAI Time Stamp every Second and a REFCLK stamp every 500 ticks to reconstruct the time. This is a more difficult format to post process but would occupy only just over 50% the data rate at the highest Event rate, allowing a longer dataset for the same memory footprint.

The FPGA logic will include a channel mask to enable/disable storage of Events on individual channels.