ACQ482ELF

16 Channel Simultaneous Analog Input Module

Product Description

- 16 channel simultaneous inputs at up to 80MHz acquisition frequency
- 14-bit resolution
- D-TACQ ELF Double Width Module (occupies 2 sites)
- Range of Input Voltages and Bandwidth Options
- Programmable High Impedance or 50 Ω termination
- High SNR typical 72dB

Digitiser Key Features

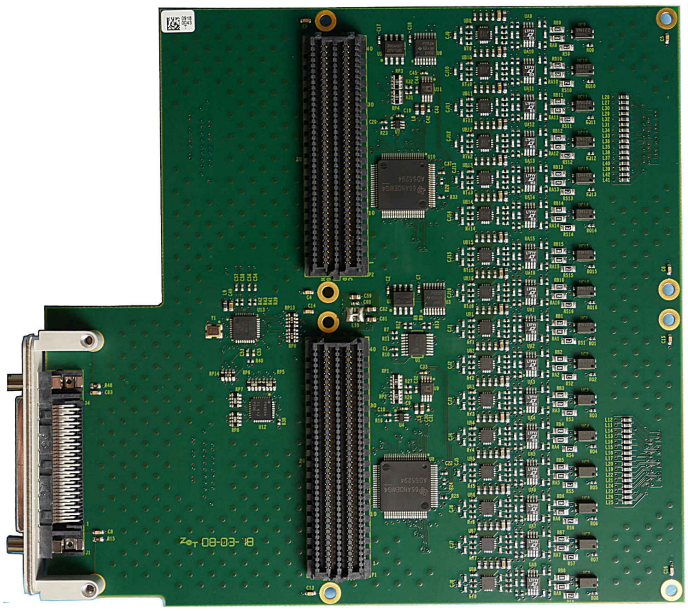
- Ideal for high speed Instrumentation applications including Radar, Radio Reflectometry, and High Speed Ultrasound
- Compatible with all D-TACQ Carriers offering up to 48 channels in a 1U 19” system
- Wide range of triggering and capture modes
- Compatible with a range of D-TACQ Breakout Panels and Termination Modules
- Internal FFC connectors for possible OEM Termination or Signal Conditioning

Platform Key Features

D-TACQ supplies a complete working Intelligent Digitizer Appliance providing :

- FPGA based system with a range of flexible and customisable features
- Microprocessor system running open source Linux
- Comprehensive API provided in Python
- Onboard EPICS IOC for rapid integration

Please contact info@d-tacq.com for details on the above system integration options.



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Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- ZYNQ : Xilinx System on Chip (SoC) + FPGA logic
- FPGA : Field Programmable Gate Array

1 Product Description

1. ACQ482ELF is an 16 channel simultaneous analog input module.
2. Standard configuration 16 channels, up to 80MSPS/channel, 14 bit resolution.
3. Differential front end, input voltage range to +/-10V.
4. Input bandwidth to 5MHz, higher for reduced voltage inputs.
5. Compatible with D-TACQ ELF sites.
6. Input connector choices “Flex Front Panel”:
   - 1 x VHDCI, 16 pairs, alternate grounds:
     - Recommended Max Bandwidth 2MHz
     - VHDCI compatible with D-TACQ range of termination panels
   - 16 x SPL. “Single Pin Lemo” (LEMO-00).
   - 16 x DPL. “Dual Pin Lemo” (LEMO-01).
   - Other input connectors possible: Please contact info@d-tacq.com
7. Module is DOUBLE WIDTH and needs two sites

1.1 Product Variants

- ACQ482ELF-16-4V-H: +/-4V input voltage range, High Bandwidth.
- ACQ482ELF-16-2V5-H: +/-2.5V input voltage range, High Bandwidth.
- ACQ482ELF-16-1V-H: +/-1V input voltage range, High Bandwidth.
- Special build due to component obsolescence:
  - ACQ482ELF-16-10V: +/-10V input voltage range, Standard Bandwidth.
  - ACQ482ELF-16-5V: +/-5V input voltage range, Standard Bandwidth.
- Special build with special component choice:
  - ACQ482ELF-16-2V5-F1: +/-2.5V input voltage range, Standard Bandwidth. High Common Mode Rejection Ratio (CMRR)

1.2 Product Overview

ACQ482ELF uses the same octal ADC subsystem used on the successful ACQ480FMC product, but provides a wider voltage range and differential input.

The product is intended to be used as an oversampling digitizer. Single, or 2 cascaded FIR digital filters provide tight control of bandwidth with strong anti-aliasing. Filtering includes both ADC based filters and FPGA based filtering in D-TACQ Carriers and covers many combinations. Please contact info@d-tacq.com for more information on this.

1.3 Applications

- Radar, Radio Reflectometry
- High speed ultrasound and diagnostics..

1.4 Replaces

- ACQ216CPCI : 16 channels x 10MSPS, replaced by 1 modules.
- ACQ132CPCI : 32 channels x 2MSPS, replaced by 2 modules.

1.5 Carrier Compatibility

The ELF module standard, based on the same front panel and connector footprint as FMC, adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends carriers based on the Xilinx ZYNQ system on chip, combining FPGA resource with a dual-core ARM Cortex A9 and gigabit Ethernet see Module Carriers.

As the ACQ482ELF is a dual site module this restricts the carrier compatibility, these include:

- D-TACQ ACQ2106 : D-TACQ 6 site ELF carrier, ZYNQ Z7030
- D-TACQ ACQ2206 : D-TACQ 6 site ELF carrier, ZYNQ Z7030
- D-TACQ ACQ1102 : D-TACQ 2 site FMC/ELF carrier, Z7030
- DAMC-FMC1Z7IO + D-TACQ ACQ400-MTCA-RTM-2 : 2 site ELF + 1 site FMC carrier, ZYNQ Z7030/7035

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

2 Physical

2.1 Board Outline

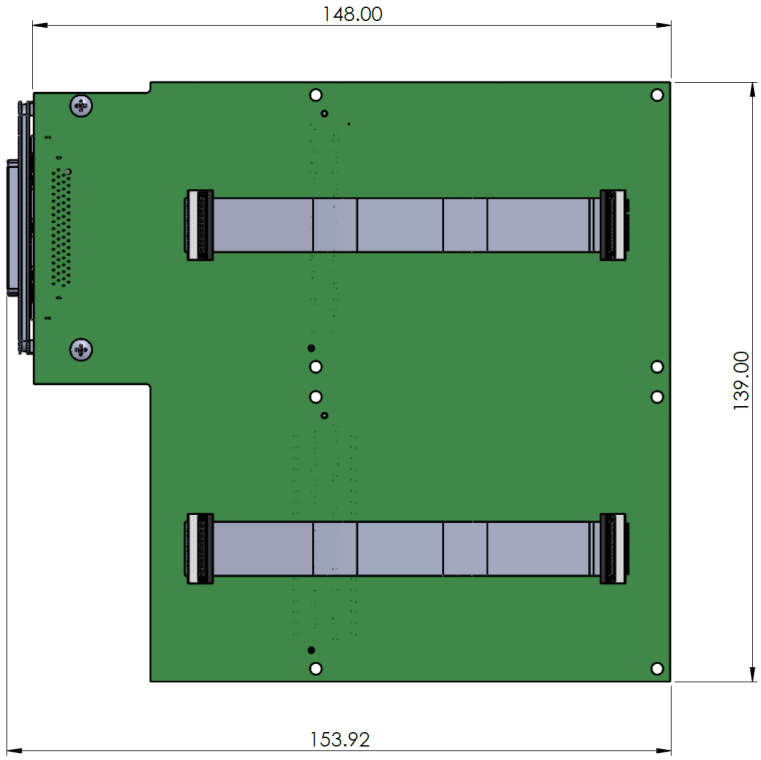

Figure 1: Board Outline

2.2 Appearance with VHDCI Connector

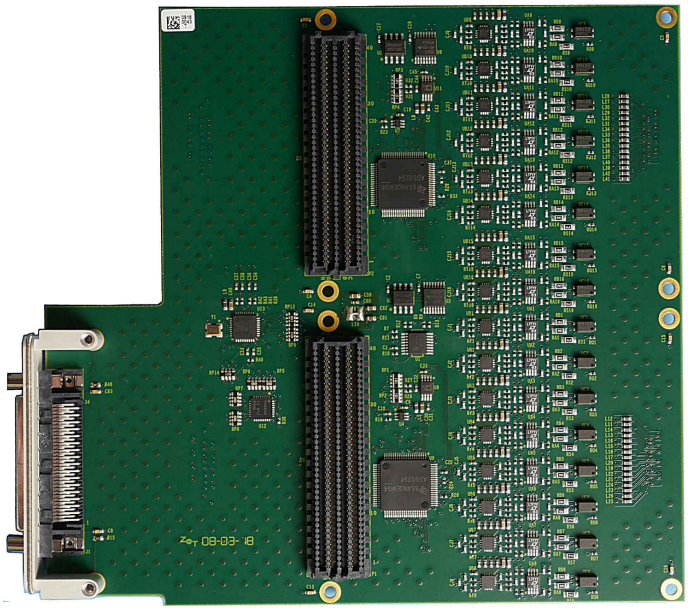

Figure 2: Board Photo

2.3 Front Panel Connectors

2.3.1 VHDCI

- 68 Pin VHDCI. Pinout compatible with D-TACQ BNCPANEL, SMAPANEL, LEMOPANEL, PTBPANEL
- For direct external cable to front panel

Pin	Function	Pin	Function
1	0V	35	0V
2	0V	36	0V
3	AI01+	37	AI01-
4	0V	38	0V
5	AI02+	39	AI02-
6	0V	40	0V
7	AI03+	41	AI03-
8	0V	42	0V
9	AI04+	43	AI04-
10	0V	44	0V
11	AI05+	45	AI05-
12	0V	46	0V
13	AI06+	47	AI06-
14	0V	48	0V
15	AI07+	49	AI07-
16	0V	50	0V
17	AI08+	51	AI08-
18	0V	52	0V
19	AI09+	53	AI09-
20	0V	54	0V
21	AI10+	55	AI10-
22	0V	56	0V-
23	AI11+	57	AI11-
24	0V	58	0V
25	AI12+	59	AI12-
26	0V	60	0V
27	AI13+	61	AI13-
28	0V	62	0V
29	AI14+	63	AI14-
30	0V	64	0V
31	AI15+	65	AI15-
32	0V	66	0V
33	AI16+	67	AI16-
34	0V	68	0V

Table 1: Front Panel VHDCI Connector Pinout

2.3.2 Flat Flexible Cable - FFC to Front Panel

- Single Pin LEMO Front Panel Adaptor
  - Centre-input +ve / shield -ve, Single Pin LEMO NIM-CAMAC 00 Series
  - Board Part EPL.00.250.NTN
  - Mating part: any 00.250 series cable connector. eg FFA.00.250.NTACxx
- Dual Pin LEMO Front Panel Adaptor
  - Differential Dual Pin LEMO 0S Series Hermaphroditic keying (half moon insert) with male pin 1

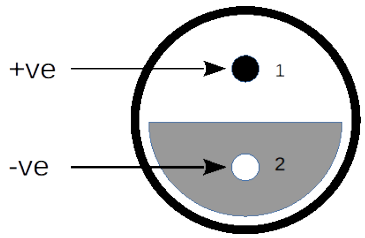

Figure 3: Dual Pin LEMO Pinout, view from Front Panel

  - Board Part ECP.0S.302.CLN
  - Mating part: any 0S.302 series cable connector. eg FFA.OS.302.CLxx
  - Optional Shield to Chassis Jumper connection on the front panel
- For custom front panel. Please contact info@d-tacq.com for details

2.3.3 Example Configuration in Carrier

The example below shows the VHDCI version fitted to a ACQ2106 Carrier

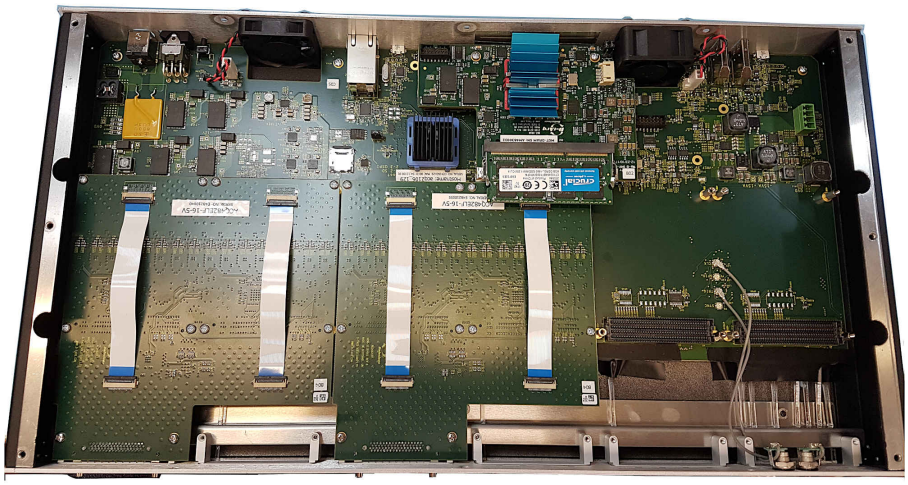

Figure 4: Example Fitted to ACQ2106 Carrier, 32 channels in 1U

3 Electrical Specification

#	Parameter	Value
1	Number of Channels	16
2	Sample Rate	Up to 80 MHz, per channel simultaneous [1]
3	Resolution	14-bit
4	Coupling	DC, Differential Input
5	Input Impedance	100 kΩ, [50 Ω software setting]
6	Input Voltage Range	±10 V ±5 V ±2.5 V ±1 V[2]
7	Input Voltage Withstand	Up to ±30 V on ±10 V version
8	Offset Error	±3 mV
9	Gain Error	±2 mV
10	INL	±2.2 LSB
11	DNL	±0.5 LSB
12	THD	80 dBc
13	SINAD	71 dBc
14	SFDR	85 dBc
15	SNR	72 dB
16	CMRR	60 dB (80 dB)[3]
17	Power BW	5 MHz @ 5 Vpp (±10 V variant) 10 MHz @ 2 Vpp (±5 V variant) 20 MHz @ 1 Vpp (-H variants)
18	Small Signal BW	20 MHz >20 MHz (-H variants)
19	Crosstalk	< 90 dB @ 100 kHz FS Input
20	Temperature Stability	< 25 ppm/°C

[1] Max ADC Frequency, decimating FIR filter reduces stored data rate. Please contact info@d-tacq.com for details
[2] See Product Variants Section 1.1
[3] On high CMRR version -F1

Table 2: ACQ482ELF Electrical Performance

4 Mechanical & Environmental Specification

#	Parameter	Value
1	Form Factor	Double width, double socket ELF
2	Power Consumption	Typical 5W, Max 7.5W
3	Environmental	0 °C - 50 °C Operational −10 °C - 85 °C Non-Operational
4	Mezzanine Socket	ELF (ULPC)

Table 3: Mechanical & Environmental Specification

Revision History

Revision	Date	Author(s)	Description
6	14/02/2020	JMcL	Product Release Version
7	31/03/2024	JMcL	Updates for latest format and latest product variants