ACQ420FMC
Product Specification

High Performance Simultaneous Data Acquisition

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1 Product Description

1. ***ACQ420FMC*** is a 4 channel simultaneous analog input module.
2. Standard configuration : 4 channels, 1000kSPS/channel.
3. Complies with *VITA57 FMC* standard, *LPC* version.
4. 2-wire Differential inputs, high quality differential amplifier front end with switched input voltage ranges.
5. Compliant with D-TACQ *ELF* sites.

1.1 Product Variants

- ***ACQ420FMC-4-1000*** : 4 channels, 16 bit resolution, 1000kSPS/channel.
- ***ACQ420FMC-4-1000-18*** : 4 channels, 18 bit resolution, 1000kSPS/channel.
- ***ACQ420FMC-4-2000*** : 4 channels, 16 bit resolution, 2000kSPS/channel.

1.2 Applications

- Instrumentation applications, control and monitoring.

1.3 Overview

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with a dual-core ARM Cortex A9 and gigabit Ethernet.

Compatible carriers include:

- D-TACQ **ACQ1001** : D-TACQ single slot FMC carrier, Z7020
- D-TACQ **ACQ1002** : D-TACQ dual slot FMC carrier, Z7020
- D-TACQ **ACQ2006** : D-TACQ 6 slot FMC carrier, Z7020
- D-TACQ **ACQ2106** : D-TACQ 6 slot FMC carrier, Z7030

- Xilinx ZC702 evaluation board with 2 FMC slots.
- Xilinx Zedboard with 1 FMC Slot.

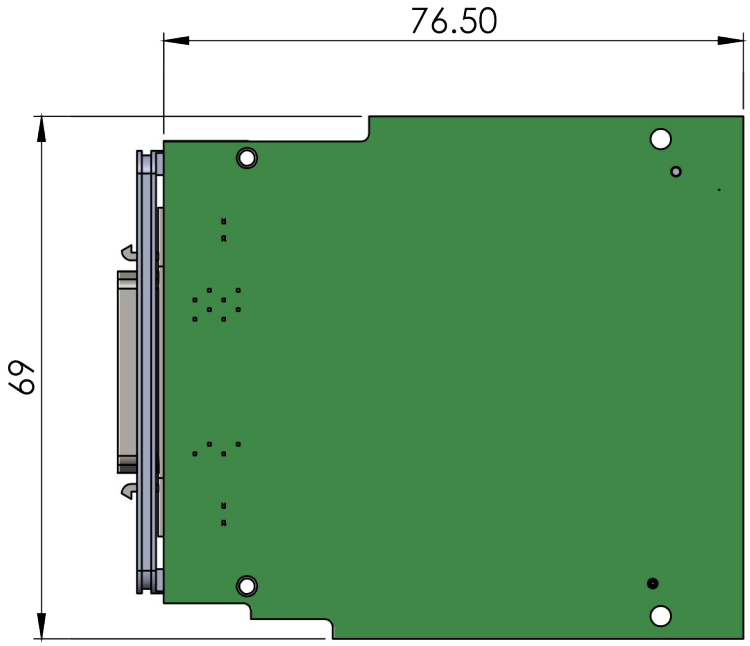
D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux. Evaluation boards are useful for evaluation, but for production use D-TACQ recommends use of a production-quality carrier such as ACQ1001.

1.4 Glossary

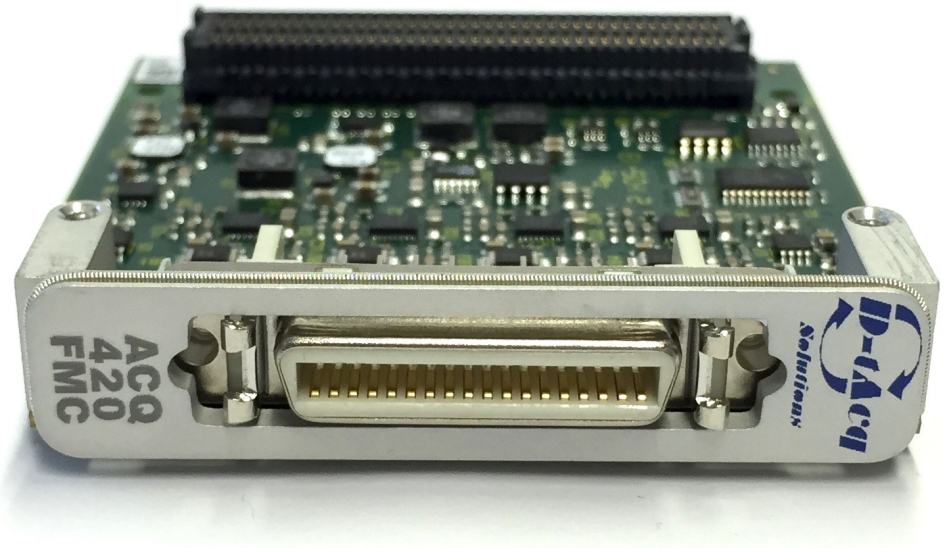
- *FMC*: VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ Soc
- *FPGA* : Field Programmable Gate Array.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC*: *FMC* Ultra low pin count (D-TACQ).
- Extended, ELF : *FMC* Extended size module (D-TACQ).

2 Physical

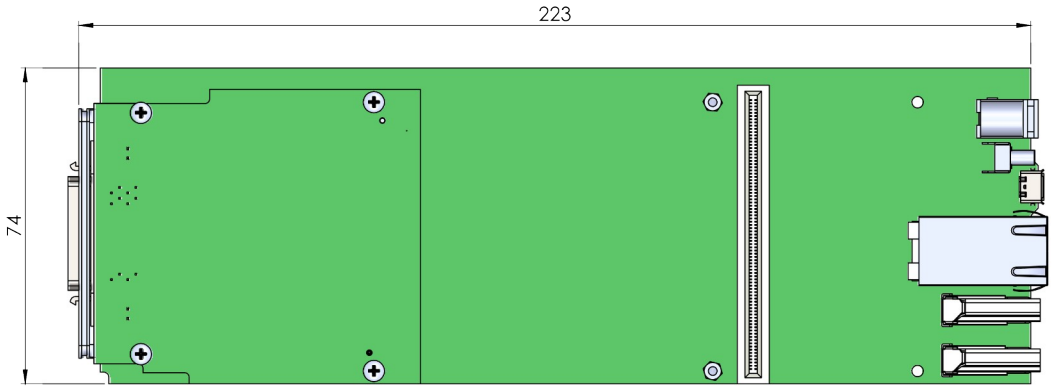
2.1 Standard FMC Module



2.2 Appearance



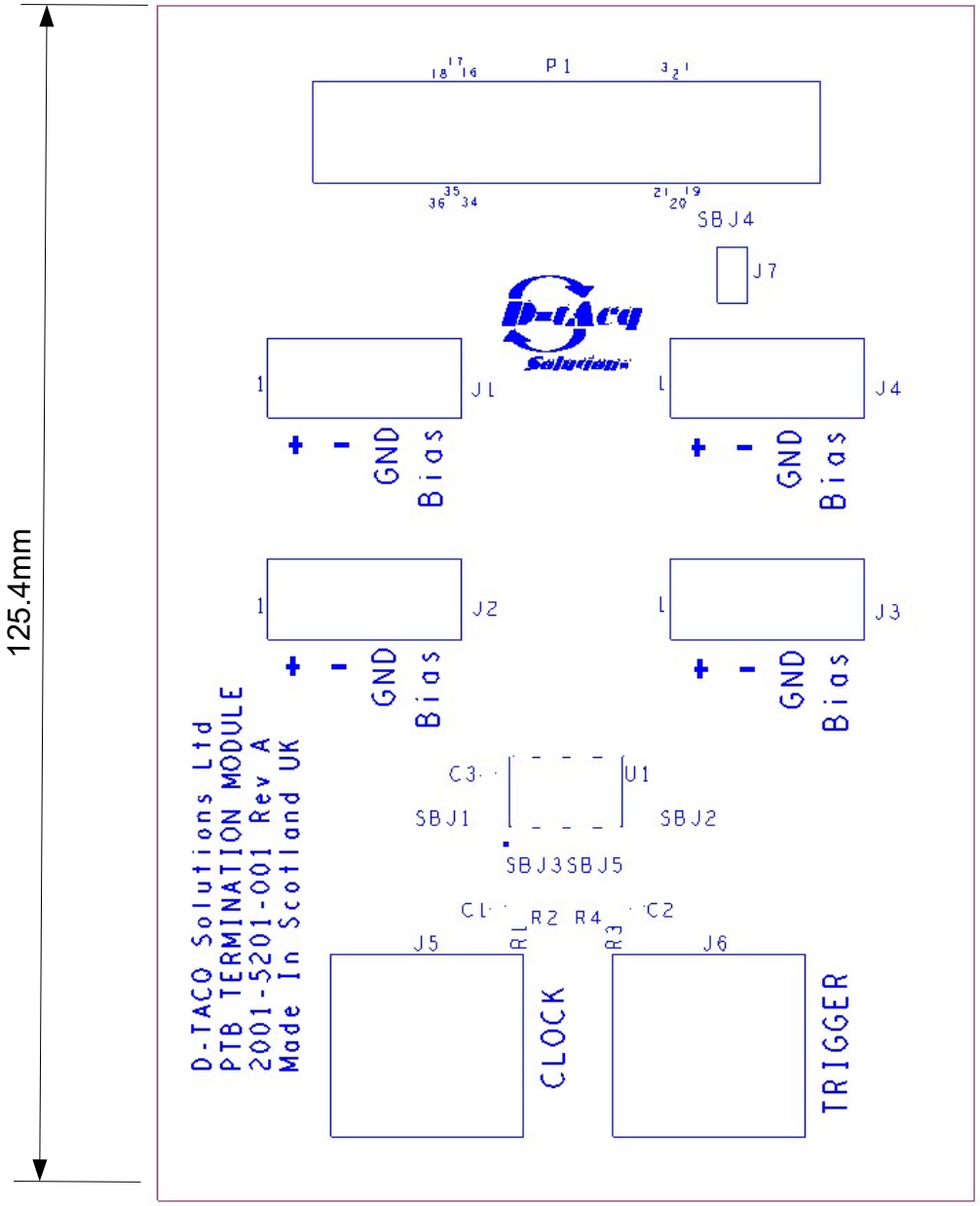
2.3 Example: Fitted to ACQ1001 Carrier



Carrier accommodates 1 x FMC e.g. ***ACQ420FMC*** or an extended size module.

2.4 ACQ420-TERM01 Termination – Physical

Optional DIN-RAIL termination accessory with 4-pin pluggable terminal blocks and opto-isolated CLK, TRG on BNC. Please contact D-TACQ for more information.



3 Interface Specification.

3.1 Front Panel Connector

- 36 Pin MDR (Centronics) 3M 10236-55G3PL
- Mating Part 3M 10136-6000EL
- Compatible cables include:
  - Videk 1082-2
- Compatible DIN-RAIL module ***ACQ420-TERM01*** available.

3.1.1 Front Panl Pinout

Pin	Function	Pin	Function
1	EXT_CLK1	19	ACCESSORY_PRESENT
2	0VD	20	0VD
3	EXT_TRIG1	21	0VD
4	0VD	22	0VD
5	+12V	23	+5VA
6	+12V	24	+5VA
7	0VA	25	0VA
8	CH_4_BIAS	26	CH_4_GND
9	CH_4+	27	CH_4-
10	0VA	28	0VA
11	CH_3_BIAS	29	CH_3_GND
12	CH_3+	30	CH_3-
13	0VA	31	0VA
14	CH_2_BIAS	32	CH_2_GND
15	CH_2+	33	CH_2-
16	0VA	34	0VA
17	CH_1_BIAS	35	CH_1_GND
18	CH_1+	36	CH_1-

3.2 FMC Connector Pinout

The ACQ420FMC module uses a LPC FMC connector with the following pin out

FMC Pin	Signal Name	Description
p_FMC_CLK0_M2C_p	FMC_ADC_CLK	Sample Clock to/from Front Panel
p_FMC_LA00_CC_p	ADC_1_CNV	Convert Pulse to ADC 1
p_FMC_LA01_CC_p	ADC_1_SCK	SPI Clock to ADC 1
p_FMC_LA02_p	ADC_3_CNV	Convert Pulse to ADC 3
p_FMC_LA03_p	ADC_1_SDO	SPI Data Out from ADC 1
p_FMC_LA04_p	ADC_3_SDO	SPI Data Out from ADC 3
p_FMC_LA05_p	ADC_2_CNV	Convert Pulse to ADC 2
p_FMC_LA06_p	FMC_OPTO_PRSNT_n	Term Module with opto-couplers present
p_FMC_LA07_p	ADC_3_SCK	SPI Clock to ADC 3
p_FMC_LA08_p	ADC_2_SCK	SPI Clock to ADC 2
p_FMC_LA09_p	ADC_2_SDO	SPI Data Out from ADC 2
p_FMC_LA10_p	FMC_ADC_CLK_DIR	Sample Clock Direction 0 = Input 1= Output
p_FMC_LA11_p	ADC_4_CNV	Convert Pulse to ADC 4
p_FMC_LA12_p	ADC_4_SCK	SPI Clock to ADC 4
p_FMC_LA13_p	FMC_ADC_TRIG	Sample Trigger to/from the Front Panel
p_FMC_LA14_p	FMC_ADC_TRIG_DIR	Sample Trigger Direction 0 = Input 1= Output
p_FMC_LA15_p	ADC_4_SDO	SPI Data Out from ADC 4
p_FMC_LA16_p	ADC_A0(0)	In-Amp ADC 1 Gain bit 0
p_FMC_LA17_CC_p	ADC_A1(0)	In-Amp ADC 1 Gain bit 1
p_FMC_LA18_CC_p	ADC_A0(1)	In-Amp ADC 2 Gain bit 0
p_FMC_LA19_p	ADC_A1(1)	In-Amp ADC 2 Gain bit 1
p_FMC_LA20_p	ADC_A0(2)	In-Amp ADC 3 Gain bit 0
p_FMC_LA21_p	ADC_A1(2)	In-Amp ADC 3 Gain bit 1
p_FMC_LA22_p	ADC_A0(3)	In-Amp ADC 4 Gain bit 0
p_FMC_LA23_p	ADC_A1(3)	In-Amp ADC 4 Gain bit 1

The ADC devices are Linear Tech LTC237X (500 kHz = LTC2377, 1000 kHz = LTC2378, 2000 kHz = LTC2380)

The In-Amp is AD8251 to set the Front End Gain

ACQ420FMC has a 24C64 Serial Prom with FRU data-
Address = 010100 GA1 GA0

ACQ420FMC also has a AD7417 Temperature Sensor on the I2C bus
Address = 001010 GA1 GA0

3.3 Example Top Level VHDL

The sample text below gives a prototype VHDL entity declaration for the FMC I/O pins of the ACQ420FMC Module. The pin naming convention on the module is as per standard FMC specification pin names.

```
--------------------------------------------------------------------------------
--                      ACQ420FMC I/Os
--------------------------------------------------------------------------------



--! Standard Libraries - numeric.std for all designs
library ieee;
use ieee.std_logic_1164.all;      -- Standard Logic Functions
use ieee.numeric_std.all;         -- Numeric Functions for Signed / Unsigned
Arithmetic

--! Xilinx Primitive Library
library UNISIM;
use UNISIM.VComponents.all;       -- Xilinx Primitives

entity ACQ420FMC_TOP is
port(
  p_FMC_CLK0_M2C_p     : inout    std_logic; --! FMC_ADC_CLK
  p_FMC_CLK0_M2C_n     : inout    std_logic; --! Not Used
  p_FMC_LA00_CC_p      : inout    std_logic; --! ADC_1_CNV
  p_FMC_LA00_CC_n      : inout    std_logic; --! Not Used
  p_FMC_LA01_CC_p      : inout    std_logic; --! ADC_1_SCK
  p_FMC_LA01_CC_n      : inout    std_logic; --! Not Used
  p_FMC_LA02_p         : inout    std_logic; --! ADC_3_CNV
  p_FMC_LA02_n         : inout    std_logic; --! Not Used
  p_FMC_LA03_p         : inout    std_logic; --! ADC_1_SDO
  p_FMC_LA03_n         : inout    std_logic; --! Not Used
  p_FMC_LA04_p         : inout    std_logic; --! ADC_3_SDO
  p_FMC_LA05_p         : inout    std_logic; --! ADC_2_CNV
  p_FMC_LA06_p         : inout    std_logic; --! FMC_OPTO_PRSNT_n
  p_FMC_LA07_p         : inout    std_logic; --! ADC_3_SCK
  p_FMC_LA08_p         : inout    std_logic; --! ADC_2_SCK
  p_FMC_LA09_p         : inout    std_logic; --! ADC_2_SDO
  p_FMC_LA10_p         : inout    std_logic; --! FMC_ADC_CLK_DIR
  p_FMC_LA11_p         : inout    std_logic; --! ADC_4_CNV
  p_FMC_LA12_p         : inout    std_logic; --! ADC_4_SCK
  p_FMC_LA13_p         : inout    std_logic; --! FMC_ADC_TRIG
  p_FMC_LA14_p         : inout    std_logic; --! FMC_ADC_TRIG_DIR
  p_FMC_LA15_p         : inout    std_logic; --! ADC_4_SDO
  p_FMC_LA16_p         : inout    std_logic; --! ADC_A0(0)
  p_FMC_LA17_CC_p      : inout    std_logic; --! ADC_A1(0)
  p_FMC_LA18_CC_p      : inout    std_logic; --! ADC_A0(1)
  p_FMC_LA19_p         : inout    std_logic; --! ADC_A1(1)
  p_FMC_LA20_p         : inout    std_logic; --! ADC_A0(2)
  p_FMC_LA21_p         : inout    std_logic; --! ADC_A1(2)
  p_FMC_LA22_p         : inout    std_logic; --! ADC_A0(3)
  p_FMC_LA23_p         : inout    std_logic  --! ADC_A1(3)
  );
end ACQ420FMC_TOP;
```

The internal names on the comments have the following definitions

---

```
-------------------------------------------------------------------------------
-- FMC pin name translation signals.
-------------------------------------------------------------------------------
signal p_ADC_CNV          : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC Convert Control
signal p_ADC_SPI_CLK      : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC SPI Clock
signal p_ADC_SDO          : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC SPI Data
signal p_ADC_A0           : std_logic_vector( 4 downto 1)       := (others => '0');
            --! AD8251 Gain Setting Address Bit 0
signal p_ADC_A1           : std_logic_vector( 4 downto 1)       := (others => '0');
            --! AD8251 Gain Setting Address Bit 1
signal p_FMC_ADC_CLK      : std_logic;
            --! Sample Clock from ACQ420FMC
signal p_FMC_ADC_TRIG     : std_logic;
            --! Trigger from ACQ420FMC
signal p_FMC_OPTO_PRSNT_n : std_logic;
            --! Accessory connected to ACQ420FMC - required for External Clock and
Trigger operation

-- Internal Names
signal ADC_CNV            : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC Convert Control
signal ADC_SPI_CLK        : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC SPI Clock
signal ADC_SDO            : std_logic_vector( 4 downto 1)       := (others => '0');
            --! ADC SPI Data
signal ADC_A0                     : std_logic_vector( 4 downto 1)       := (others =>
'0');       --! AD8251 Gain Setting Address Bit 0
signal ADC_A1                     : std_logic_vector( 4 downto 1)       := (others =>
'0');       --! AD8251 Gain Setting Address Bit 1
signal FMC_ADC_CLK        : std_logic;
            --! Sample Clock from ACQ420FMC
signal FMC_ADC_TRIG               : std_logic;
                  --! Trigger from ACQ420FMC
signal FMC_OPTO_PRSNT_n   : std_logic;
            --! Accessory connected to ACQ420FMC - required for External Clock and
Trigger operation
signal FMC_IO_BUS         : std_logic_vector(3 downto 0) := (others => '0');
      --! FMC IO Controls (CLOCK_DAT,CLOCK_DIR,TRIG_DAT,TRIG_DIR)
```

The 4 bit bus definitions are for the 4 ADC devices on the ACQ420FMC, each device has a full SPI bus, for simultaneous capture all devices should be driven from the same Convert and Clock sources.

The AD8251 PGAs have a 2 bit control shown above as A1 and A0. Therefore for ADC 4 the PGA controls would be

ADC_A1(4)	ADC_A0(4)	Gain
0	0	x1
0	1	x2
1	0	x4
1	1	x8

4 ACQ420FMC Electrical Specification.

#	Parameter	Value
1	Number of Channels	4
2	Sample Rate	-500: 500 kHz -1000: 1 MHz -2000: 2 MHz per channel simultaneous
3	Resolution	16 bits [18 bit]
4	Coupling	DC, Differential Input
5	Input Impedance	1 MΩ
6	Input Voltage Range Standard (1,2,4,8) High Gain (1,10,100,1000)	Software selectable ranges. ±10V,±5V,±2.5V,±1.25V ±10V,±1V,±100mV,±10mV
7	Input Voltage Withstand	±30V
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	16 bit ±0.2 LSB 18 bit ±0.5 LSB
11	DNL	16 bit ±0.1 LSB 18 bit ±0.1 LSB
12	CMRR	>80dB FS @ 1 kHz
13	THD	-98 dB* at gain 1
14	SINAD	-93 dB* at gain 1
15	SFDR	100 dBc*
16	SNR Gain *1 SNR Gain *2 SNR Gain *4 SNR Gain *8	94 dB* 94 dB* 92 dB* 90 dB*
17	Power BW (-3 dB)**	-500: 250 kHz -1000: 450 kHz -2000: 450 kHz
18	Small Signal BW**	-500: 250 kHz -1000: 500 kHz -2000: 800 kHz
19	Crosstalk	<90 dB @ 1 kHz FS Input
20	Temperature Stability	<25 ppm/C

Typical values

* Typical values measured at full scale with a 9.76kHz input
** Bandwidth is reduced in High Gain configuration. Contact factory for details

5 ACQ420FMC Mechanical and Environmental Specification

#	Parameter	Value
1	Form Factor	Standard FMC
2	Power source	External DC 12V, 150mA External DC 3.3V, 75mA
3	Environmental	0°C-50°C Operational -10°C-85°C Non-Operational
4	FMC Socket	Standard FMC, Low Pin Count LPC
5	Digital Signal IO	CLK, TRG inputs 5V TTL