BOLO8BLF Product Specification

High Performance Simultaneous Data Acquisition

Contents

Revision History

Revision	Date	Author(s)	Description
1	19/02/2015	-	Created
2	18/07/2010	-	-
3	26/10/2023	SR	Updated to new style

Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- Xilinx ZYNQ System on Chip (SoC)
- FPGA : Field Programmable Gate Array

1 Product Description

1. BOLO8BLF is an 8 channel simultaneous analog I/O module for controlling and measuring bolometers with typical resistance of 1.2 kΩ
2. Analog Inputs: 8 channels, 16-bit resolution, 1000 kSPS/channel
3. Differential bridge excitation common to all channels: 1000 kSPS, 16-bit DAC. Typical output is ±10V @ 20kHz
4. Calibration
    - 8 channel single-ended Offset DAC, 16-bit resolution
    - Current Measurement ADC at 12-bit resolution, 200 kSPS typical use case
5. Extended module with FMC connector. 4x RJ45 connectors for ease of connection; 2 bolometer foils per connector
6. Differential inputs, high quality differential amplifier front end with switched input voltage ranges

1.1 Carrier Compatibility

The BLF module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with ARM CPU and Gigabit Ethernet.

The BLF module standard is a D-TACQ standard and is compatible with only D-TACQ Carriers.

Compatible carriers include:

- D-TACQ ACQ2106 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ2206 : D-TACQ 6 slot FMC carrier, Z7030

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

2 Physical

2.1 Board Outline - BLF Extended FMC Module

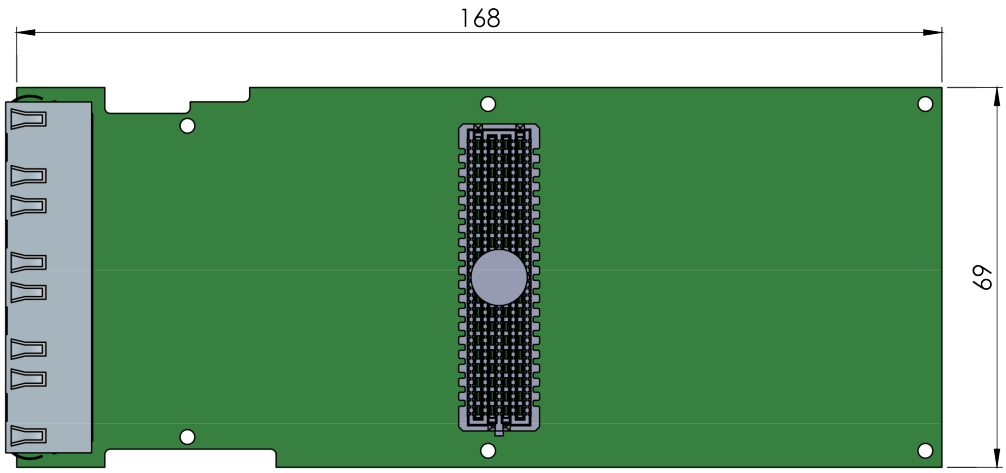
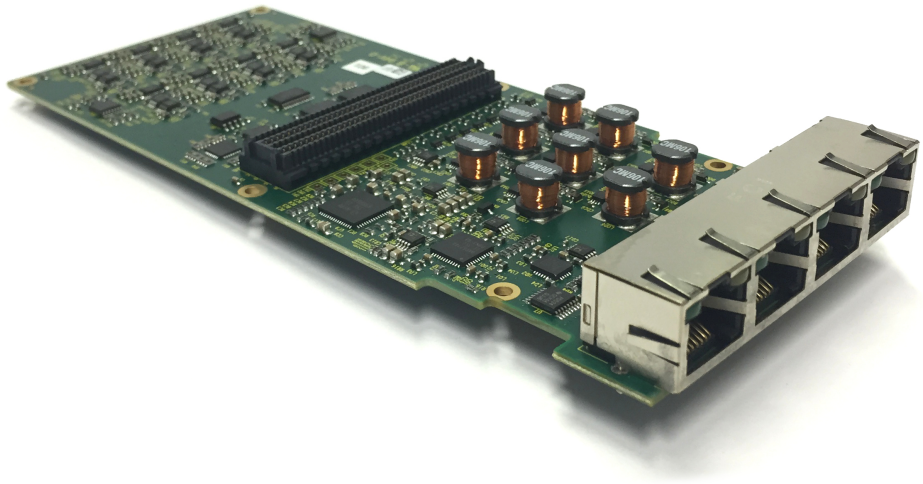


Figure 1: Board Outline

2.2 Appearance



(a) Mezzanine

(b) 6 x BOLO8BLF in ACQ2006 Carrier - 48 Channel System

Figure 2: Board Appearance

2.3 Front Panel Connectors

2.3.1 RJ45

- 4 x RJ45 connectors
- Input/Output wiring is configured to use standard Ethernet cable differential pairing for ease of wiring
- The pinout for all 4 RJ45 connectors is identical
- The bolometer bridge must be connected as indicated in Table 1 and Figure 3 below.
- The BOLO8 has eight channels of I/O on four RJ45 connectors
  - 2 channels per connector

Pin	Function
1	+Channel A In (+Offset DAC Out)
2	-Channel A In (+Offset DAC Out)
3	+Channel A Excitation Out
4	-Channel B Excitation Out
5	+Channel B Excitation Out
6	-Channel A Excitation Out
7	+Channel B In (+Offset DAC Out)
8	-Channel B In (-Offset DAC Out)

Table 1: BOLO8BLF Front Panel RJ45 Pinout

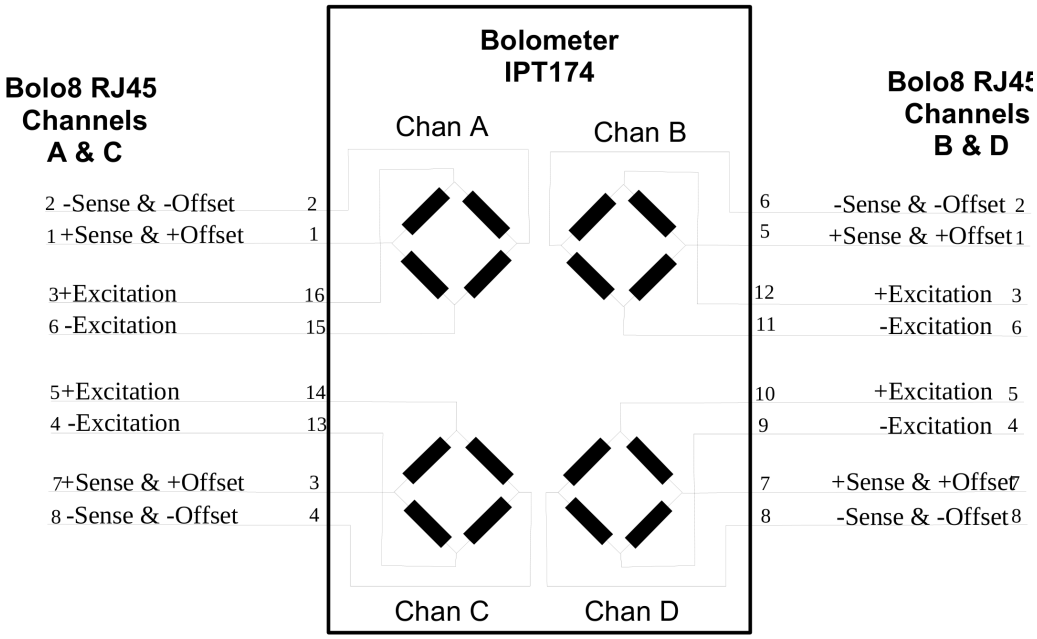


Figure 3: Bolometer Foil Connections

If the connection to the bolometer head is made using RJ45 cable assemblies be aware of the wire colour coding differences between 568A and 568B standards.

(a) RJ45 Plug - TIA/EIA 568A (b) RJ45 Plug - TIA/EIA 568B

Figure 4: RJ45 Wiring Standards

Failure to connect the BOLO8 correctly to the bolometer bridge may cause damage to the BOLO8 board. This can be avoided by ensuring no short circuits are made between any of the BOLO8 RJ45 connections and ensuring that the bridge connections are isolated from power supplies and ground. In addition, the minimum resistance between any two legs of the bridge must not be less than 100 Ω.

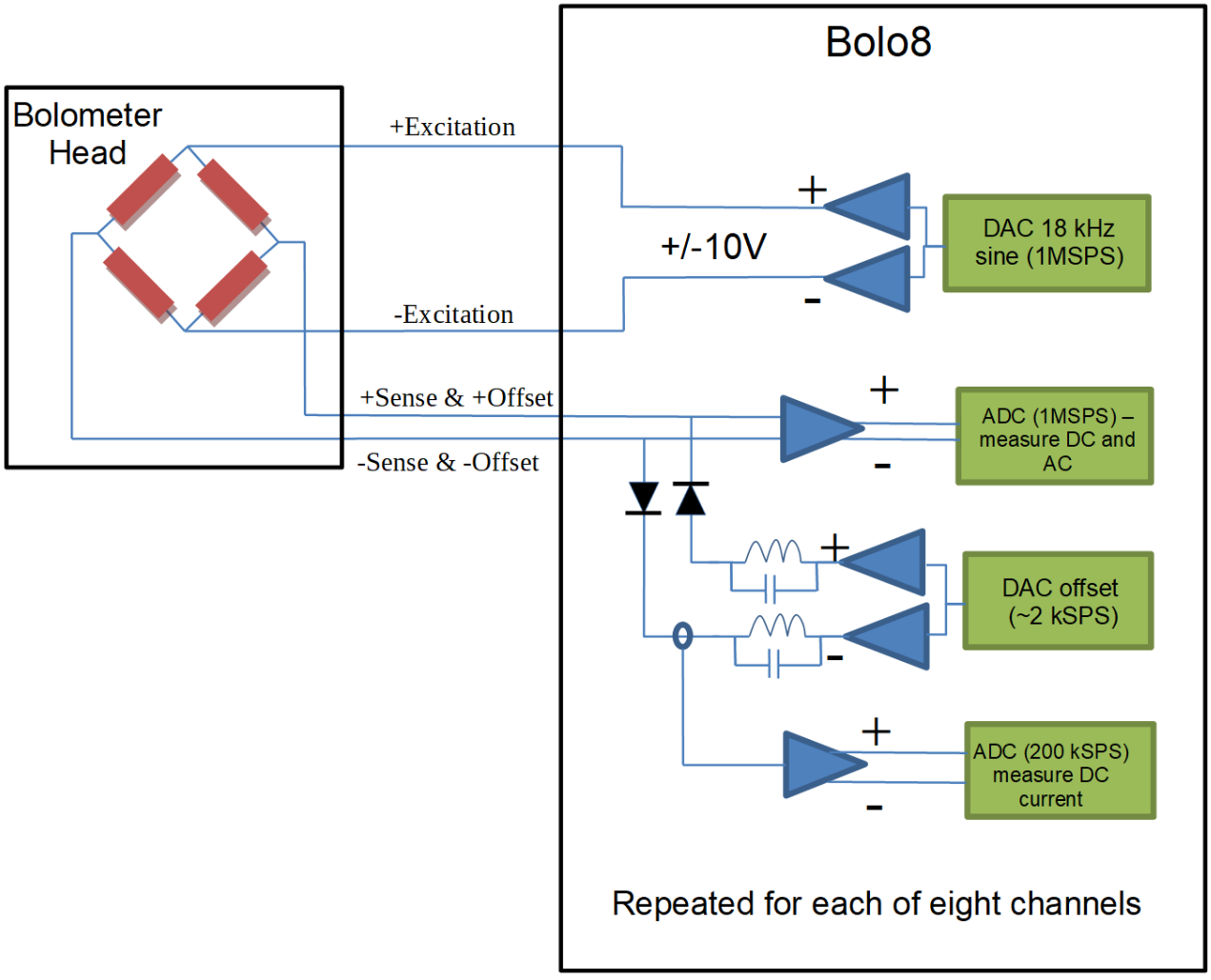


Figure 5: BOLO8BLF Block Diagram with RJ45 wiring

3 Theory of Operation

The main DAC excites all eight bolometer bridges. Each bolometer has an individual ADC to digitise the incoming data.

Calibration is performed by forward-biasing the Offset DACs and measuring the resulting current. A 20kHz Bandstop filter separates the offset DAC from the excitation.

A comprehensive FPGA control personality was developed at CCFE and is available from D-TACQ.

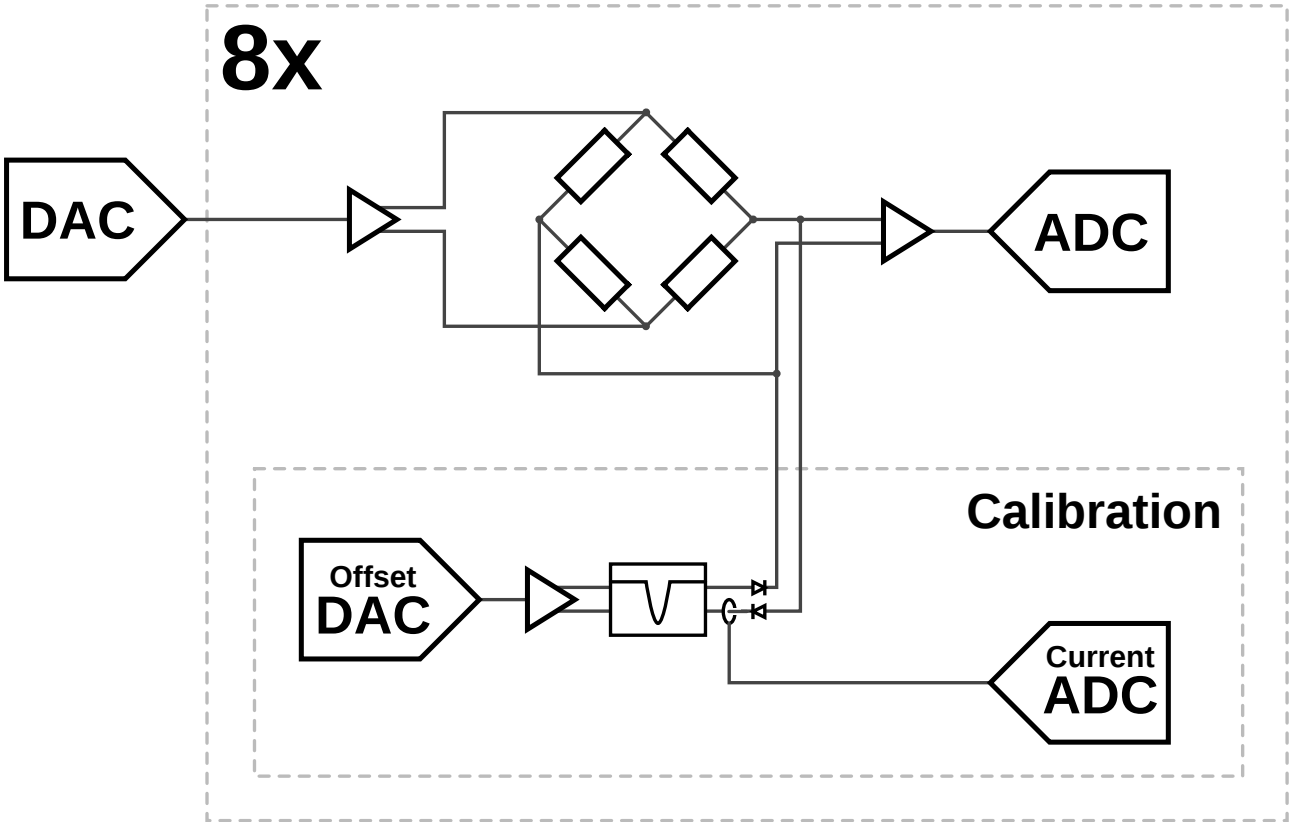


Figure 6: BOLO8BLF Block Diagram - Bridge is shown for reference

4 Electrical Specification

4.1 Main ADC

#	Parameter	Value
1	Number of Channels	8
2	Sample Rate	Up to 1000 kHz, per channel simultaneous
3	Resolution	16-bit
4	Coupling	DC, Differential Input
5	Input Voltage Range	±10V ±5V ±2.5V ±1.25V software selectable ranges
6	INL	16-bit ±0.5 LSB
7	DNL	16-bit ±0.1 LSB
8	Full Power BW	250 kHz
9	Temperature Stability	< 25 ppm/°C

Table 2: BOLO8BLF Main ADC Electrical Performance

4.2 Main (Excite) DAC

#	Parameter	Value
1	Number of Channels	1 DAC drives 8 amplifiers for the 8 bolometer channels
2	Update Rate	Up to 1000 kHz
3	Resolution	16-bit
4	Coupling	DC, Differential Output
5	Per-Channel Max. output current	20 mA, minimum bridge impedance 100 Ω
6	Output Voltage Range	±10V
7	Output Impedance	33 Ω
8	INL	±2 LSB
9	DNL	±1 LSB
10	Full Power BW	20 kHz - matches Band Stop Filter on Offset DACs
11	Temperature Stability	< 25 ppm/°C

Table 3: BOLO8BLF Main DAC Electrical Performance

4.3 Current ADC

#	Parameter	Value
1	Number of Channels	8
2	Sample Rate	Up to 200 kHz, per channel simultaneous
3	Resolution	12-bit [1]
4	Coupling	DC, Single-ended Input
5	Input Impedance	1 MΩ
6	Input Current Range	±20 mA
7	INL	±0.2 LSB typical
8	DNL	±0.2 LSB typical
9	Temperature Stability	< 25 ppm/°C

[1] Prior to component shortages circa 2023, this was a 16-bit version of the same ADC. Board population may vary with component availability.

Table 4: BOLO8BLF Current ADC Electrical Performance

4.4 Offset DAC

#	Parameter	Value
1	Number of Channels	8
2	Update Rate	Up to 2 kHz, per channel simultaneous
3	Resolution	16-bit
4	Coupling	DC, Differential Output
5	Per-Channel Max. output current	20 mA, minimum bridge impedance 100 Ω
6	Output Voltage Range	±7.5V
7	Output Impedance	33 Ω
8	INL	±4 LSB
9	DNL	±1 LSB
10	Full Power BW	1 kHz
11	Temperature Stability	< 25 ppm/°C

Table 5: BOLO8BLF Offset DAC Electrical Performance

5 Mechanical & Environmental Specification

#	Parameter	Value
1	Form Factor	Standard BLF
2	Power Consumption	Typical 11 W
3	Environmental	0 °C - 50 °C Operational −10 °C - 85 °C Non-Operational
4	Mezzanine Socket	ELF (ULPC)

Table 6: Mechanical & Environmental Specification